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December 22,1981

To: Dave Chandler
From: Dave Hostetler

Subj: Dear Santa, for Christmas please bring us a uP design project complete with micro-code and writeable control store...Thanks, GI Design Staff...PS If it also does graphics our management and customers will be happy too.

...A Critique of the GI Advanced Video Processor DOS

The following is a personal evaluation of the recently received Design Objective Specification for GI's AY-3-89000 Advanced Video Processor. I had expected this document to be a specific and detailed solution to the specific problem of Intellivision II graphics. Through the summer and early fall we had a number of two day meetings with members of the GI and APH technical staffs to discuss directions, problems and ideas relating to this development. I knew that we would have differences with the document, but hoped that it would form a base to change and improve to arrive at an early 1982 definition to build the remaining hardware and software around.

My expectations and hopes have not been meet. The solution is general; GI is trying to kill several birds with one stone. The DOS is not detailed; the proposed IC is very large and complicated (part of being general) and it will take some time to fully think out and define the details.

GI has a number of fingers in the future pie. They are working with Jerrold to develop a Home Cable Terminal that would do videotex type applications over the two way cable systems that are coming. They are working with others (Plessy I believe) to develop terminals to work with Prestel and its variations both here and abroad. What makes it possible to have one IC that does all this and games as well? A uP of course!

GI has tried from the beginning to convince us that a special, custom uP would be desirable for our project. The idea was evaluated by Mattel and in discussions GI became convinced of our resolve to use a standard uP. It came as a bit of a surprise to see the DOS presenting a 24-bit uP as the base of the graphic interface IC. To me it appears that someone at GI is looking for a good excuse to design an advanced uP. It is hard to blame them; they have designed uPs in the past and it looks as if they might miss the chance to try one this generation. As they say, "use it or lose it".

What are the advantages and disadvantages of this generalized approach? For GI some of the advantages are: One design serves many markets, they keep their hand in on uP design and modification of the programming will allow a simplified "one chip" terminal. Advantages to Mattel are in the area of flexibility which will allow unforseen problems to be overcome more easily or new presentation ideas to be implemented. Since I believe that home terminals (banking, Videotex, etc.) are direct competition to some aspects Intellivision II, we would be working with a vendor that will likely become a direct competitor in the marketplace. Further disadvantages to Mattel are the larger chip size and much longer development time that the uP approach will require.

For size, GI simply says, "Currently greater than 64 pins."; I count 80 before even starting on major details, much less minor ones. National Semiconductor has quoted 250 man-years development time to date on the NS16000 and it isn't in full production yet. If we assume that the 24-bit machine that GI wants for their Video Processor IC is only half as complicated, I wonder where the 125 man-years will come from in the next 1.5 years (I figure we need production parts by mid-'83 to see Mattel production by early-'84). My calculator says 83 people (sects & clerks included) for that year and a half; even if you cut that in half GI could never staff it. If you give them another year or year and a half, it looks more possible. If they cut corners and manage it sooner, what will give? They could have hardware or software bugs; but more likely, they would not effectively use the capabilities of the technique.

To sum, I believe that the risk is great and the potential rewards are few. In developing my ideas for a Mattel Advanced Graphic Interface Circuit (MAGIC), I worried as it grew ever larger; GI has at least eased that somewhat, they have totally eclipsed MAGIC in size. A last image occurs to me: As I move down Main Street towards Tomorrowland, a bus marked GI rushes past. But wait, they missed the turn and zoom straight ahead over the drawbridge and into the castle. Will they get their driver straightened out and get to Tomorrowland before the party is over?

REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP

DESIGN OBJECTIVE SPECIFICATION

AY-3-89000

ADVANCED VIDEO PROCESSOR

SHEET													
LAST REV													

SHEET													
LAST REV													

DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT MICROELECTRONICS GROUP

TITLE DESIGN OBJECTIVE SPECIFICATION FOR
AY-3-89000 ADVANCED VIDEO PROCESSOR

PLANT

MODULE

OPERATION

SHEET 1 OF

SPEC. NO. REV

	WRITTEN	APPROVED
BY		

Purpose

This document introduces a high performance video processor circuit (VP) which may be connected to the bus organization of a variety of standard microprocessors. The video interface circuit directly supports standard ROM and dynamic RAM memory and performs a memory management function in support of the selected microprocessor.

Scope

A D.O.S. usually describes the internal functional characteristics of a chip in great detail and considers the external world only by provision of simple timing diagrams and specific values assigned to key edge conditions.

This information is important and helps adequately document the link between a customer/marketing definition, and the engineers interpretation of the application design.

For many applications the D.O.S. is limited to addressing only one major logical function and all involved parties can reach an early understanding of the subtilties involved in the design.

In the case of a video processor chip, it is essential to consider the wider aspects of the global system implementation. The video processor circuit performs multiple, complex, high speed operations. While in reality, it is only the "silicon visual port" for the main system microprocessor, it often dictates far more stringent conditions upon the ultimate performance of all system components, including ROM, RAM and other expansion interface chips. Indeed an advanced video processor circuit can be considerably more complex in its internal logic implementation than that required by the latest 16 bit microprocessors.

This D.O.S. provides a preliminary definition of a video processor circuit which has been optimized around the "card" approach to background display construction.

Preview

The proposed video processor circuit contains several separate but mutually supportive functional elements. The design is completely modular and individual blocks may be selected on a mix and match basis to produce other members of a family of video processor designs.

From our STIC I experience it is apparent that an object oriented foreground structure provides optimal software efficiency. In support of this architecture customized concurrent hardware must be available to provide the high processing speed that is dictated by the asynchronous operation of the foreground display.

To augment our STIC I foreground capability it is proposed that the control logic for sixteen independent objects will be available on the chip. These objects will be reusable in two ways, either through reinitialization via the system microprocessor or by using the automatic reuse feature provided by the chip.

The "background" display facility will be considerably enhanced with many new features available. The major upgrade of background facilities is provided through an architectural implementation which closely resembles an advanced 16 bit microprocessor. A rich selection of object construction definitions are available using a selection of alternative modes. This architectural technique provides important expansion flexibility by permitting redefinition of the object construction codes through reprogramming of the instruction decoder which operates upon the background definition lists.

System Overview

The AY-3-89000 is an Advanced Video Processor, combining the flexibility of a specialized Graphics Processor in conjunction with high speed dedicated logic areas, to provide the ultimate "card" based solution to text and computer generated graphics.

The important evolution of this design over contemporary architectures is based upon a unique dual functionality. During the visible display period, the device supports high speed, synchronous access to areas of external memory. The attributes and dot patterns are fetched to create complex text and graphic displays. During the vertical retrace, the device behaves as an advanced 16 bit microprocessor executing an on-chip, firmware graphic compiler.

Communication between the system CPU and the Video Processor (VP) being in functional or logical terms, greatly unburdens the "housekeeping" tasks to be performed by the system CPU. These functional entities deal with objects, the links required to create objects, or the required manipulations to be performed on them. The system CPU prepared "functional" program can be self-contained such that the VP may sustain itself independently. External resource requests are embedded within the structure of this functional program.

Through its capability of detecting "touches" and "collisions" between objects, the VP, with the assistance of the execution sequence specified in the system CPU supplied program, can reorganize the definition of objects, relocate them, link one or more, perform operations on them and eventually create the Display Descriptor List, in preparation for the VP to assume the role of displaying the dot patterns with all their specified attributes. In effect,the VP "compiles" a Descriptor list during the frame flyback, which it uses in real time, over the active display period.

It is the intention that enough intelligence be incorporated in the system CPU supplied program such that the VP in conjunction with its "task prioritizer", can inform the CPU of the status of all listed tasks and request additional resources from an external process. The complexity of the game sequence and the amount of processing to be performed by the CPU to interface with the user and the outside world determines the index of "task sharing" between the CPU and the VP.

This advanced architecture supports 3 "forms of life".

- A text based system with DRCS, Mosaic and Bit map graphics capable of supporting 40/64/80 characters per row, animation and cartoon type displays. This configuration provides a powerful tool for business/personal applications, besides being A.T.&T. and Prestel compatible.

- A very powerful "games-oriented" system that can support 16 reuseable moving objects,320x192 Resolution, 16 selectable colors, variable sized cards, multiple colors within a card, X&Y zoom, row and frame scrolling, perspective vision, multiple video planes, etc., etc., etc. - all with minimal overhead on the CPU.

- A very Intelligent Terminal, that assisted by the processing power of the CPU can support different protocols at the Link and Transport layer.

Protocol		Configuration
- Local & Metro-Net	-	2 way cable
- Didon	-	1 way broadcast
- Standard ASC11 formatting	-	2 way telephone
- Specialized code compressed data like that used in PICTURE PRESTEL	-	Intelligent photographic transmission

The VP, through its instruction set will be able to support TELIDON type geometric primitives as well as performing operations on them.

Additional Comments

1. An optimium instruction set will be designed to give enough flexibility for the CPU to generate optimized intermediate code. At the same time the instruction repertoire should not slow down the execution rate of this universal video processor.

2. During the display period, the VP, besides fetching the dot patterns and its attributes from external memory in a sequential manner, is also making "calls" to object definitions. As in normal subroutine calls, these can be nested, so that complex objects can be created as a sequence of links to less complex objects. In this regard the machine operates non-sequentially.

3. Since the VP provides transparent Dynamic RAM refresh, it is logical to incorporate the function of a Memory Manager as well. Being a non-paged, non-segmented architecture, the Memory Manager supports symbolic addressing and in effect will be the only piece of logic that is aware of the physical position of any section of code.

4. All communication between the CPU and memory takes place through the VP, which in effect,provides an extension port for receiving and transmitting messages to or from memory. Even during peak system memory utilization by the VP, the pipeline of the architecture permits transparent sychronous communication between the CPU or the processor section of the VP and memory. All bus conflicts are handled by the CPU which always has unconditional control over bus usage. The VP can be programmed to interface to a range of bus configurations.

Recommendation

A MC68000 or a CP16000 would handsomely fit the requirements of a sophisticated CPU to control this Video Processor. It is safe to assume that for any conceivable system configuration required for a low cost solution,either of the above mentioned processors, with the unique architecture of the AY-3-89000,provides a powerful 2 chip system solution (besides standard memory).

System Features

1. Programmable interface to standard 8 bit and 16 bit microprocessors.

2. 16 reusable, coordinate positioned foreground objects.

3. Two independent background planes of 40x24 characters each.

4. Two independent video outputs. (Programmable selection from the internal multi path video signals).

5. Capability to support 40/64/80 character displays.

6. NTSC and PAL compatible composite video.

7. Direct RGB drive available through digitally coded primary color pairs.

8. Lock to real time video - broadcast, video disc or tape system.

9. Interlace and non interlace capability.

10. 16 independent colors selectable from RAM based color palette.

11. Transparent refresh of both 16K and 65K dynamic RAM

12. 16M words absolute memory capacity.

13. 24 bit address bus.

14. 16 bit data bus.

Electrical Characteristics

Operating Temperature	0°C to +80°C
Supply Voltage	VCC = 5V ± 0.25V
Clock Input	14.3MHz i.e., 4xNTSC chroma
External Memory	200nsec cycle time
Pin Configuration	Currently greater than 64 pins.

Background Facilities

Two duplicated resources are provided, the following information refers to the common facilities of each single resource.

1. On chip line buffer, 40x16
2. Following row attributes fetched during flyback line
3. Selectable card width 4, 6, 8, 16 pixels (8 is most common implementation)
4. Multiple colors on a single card; 2, 4, 8 (4 is most common implementation)
5. Character pattern available from system ROM or RAM memory space
6. Uniform non paged, non segmented architecture.
7. Multiple descriptor definition with a selectable decoding structure.
8. X and Y card scroll on individual rows.
9. Ability to dynamically redefine start of screen image and visible part of system memory.
10. Perspective feature
11. Two independent video outputs
12. Transparent

Detailed Explanation

1. Current Line Buffer 40x16

This RAM memory performs the function of on chip storage of the forty 16 bit card descriptor words which specify the character selection and color definition within each card. The forty character buffer is loaded during the first line of each background row by performing a complete cycle steal DMA of the system processor.

2. Following row attributes fetched during line flyback.

The general row attributes define card height, width, X and Y offset, color palette selection and current character descriptor instruction decoding set. This area of control RAM is loaded during the line flyback preceeding the first active line of each character row.

Currently only one row attribute fetch is performed for each visible row. Future study should ascertain if any advantage can be gained by modifying the row attributes within any current row.

3. Selectable card width 4, 6, 8, 16 pixels.

The standard selection would be the 8 pixel card.

This definition currently applies to each card. The invocation of selectable card width is available under several different operational conditions.

In general the row attributes specify a common definition for all cards on that row, but under some conditions each card may be separately programmed via its own character descriptor.

The 16 pixel wide card occupies twice the horizontal width of the 4 and 8 pixel cards.

4. Multiple colors on a single card

The background descriptor word is formatted similar to a microprocessor instruction code, i.e., the 16 bit word is segmented into a number of different fields with each field organized as the select code for an appropriate function.

The system operates under an extensive instruction repertoire (well beyond the control of a single 16 bit word). To minimize requirement, selection of the appropriate graphic instruction set is specified within the row attribute set loaded during the line flyback period.

The three major color modes are:

1. Two defined colors per card
2. Four defined colors per card, (not available on 16 bit card).
3. One of eight color mode for each pixel of the 2 pixel wide card.

Note: During development we may choose to implement a 24 bit descriptor buffer and this would further expand the color and pattern options available within each card.

5. Character pattern in ROM or RAM memory

Unlike STIC I, the character descriptor code is not limited to the definition of an absolute system address. Within this video processor chip the character address value is used as the algebraic offset to be combined with the contents of one of four index registers. The appropriate index register is selected via two bits of the appropriate descriptor word.

Note: The initial index register definition considers a 24 bit implementation. If speed is a limiting factor the lower bits will be zeroed and a segmeneted structure implemented.

6. Uniform, non paged system architecture

When accessed by the system microprocessor, the total memory space, including executive ROM, data RAM, graphic patterns and video processor registers, are always available, and may be accessed by an microprocessor instruction without time or address location restrictions.

The total address capacity of the system is currently 24 bits or 16 megawords of memory space. The definition of a "word" will depend upon the organization of the selected microprocessor and may be 8 bit or 16 bit configuration. The selection of microprocessor may also dictate that less than a 24 bit address bus is supported due to limitations imposed by the processor.

7. Multiple descriptor definition with selectable decoding structure

Video systems encompass several end use applications including text, line or block graphics, complex cartoon type images, animation effects and realistic digitally generated "photographic" images.

Each of these applications may be addressed through a multiplicity of different optimized architectures. Text and text-oriented operations tend to be high density, static displays requiring relatively few computations to be performed on them on the frame flyback to maintain a dynamic display. On the other hand, in animated object oriented displays (i.e. cartoon), there are a limited number of characters, but each requires complex color selection, variable card size and extensive attributes. This requires complex linked structures for object creation allowing macro operations to be performed on these objects to create sophisticated computer generated graphics.

The selection and control of all desired features which must be available within a universal video generator solution, is not possible using only a single 16 bit graphic instruction word. The proposed solution is that several optimized "instruction sets" are defined and all are stored within the microcode ROM resident within the video generator chip, (currently three sets are required). The appropriate instruction set may be selected either through the line flyback accessed attribute data, or by executing one of the special link instructions which are used to change between instruction sets and which may be invoked through the normal background character descriptor list.

The final definition and coding of each instruction has yet to be assigned but the grouping will tend to segregate between text,bit pattern graphics and geometric generated graphics.

It may be possible to refine the structure to include only two alternative instruction sets.

It may also be desirable to include a small area of RAM in support of the microcode ROM with the objective of providing an area of "writeable control store". This is a feature common to most advanced computer architectures. A writeable control store provides the ideal facility of permitting redefinition of the instruction set during program run time. This technique allows the skilled user to increase the throughput of the system at critical areas of the applications program.

8. X and Y Scroll on Individual Rows

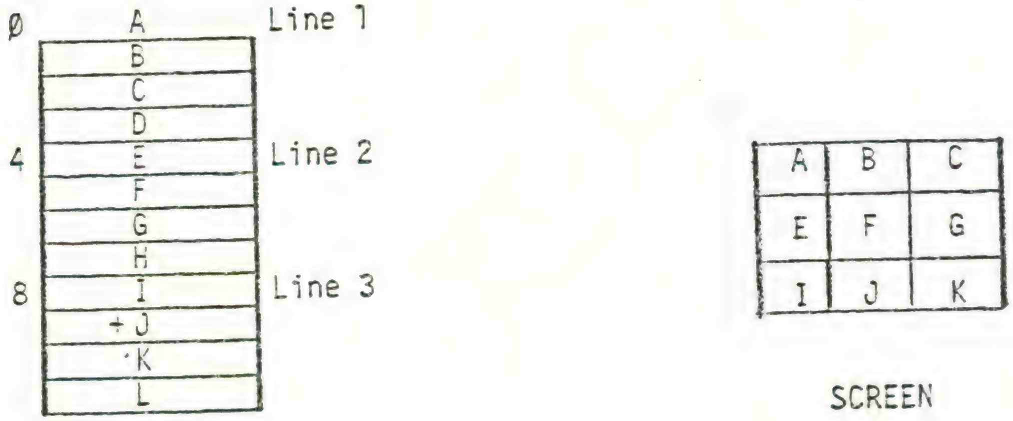
The row attribute list which is accessed during line flyback time contains definition codes specifying the individual X and Y offset for the following character row. This is an integer value which is currently unsigned in X.

The use of the multiple scroll feature allows an effective perspective zoom to be implemented in conjunction with a rate multiplier control of card clock rates.

9. Dynamically redefine start of screen image and visible part of system memory.

All current video systems utilize the system RAM as a contiguous block with each word dedicated to sequential card positions on the screen.

It is proposed that this video processor uses an indirect pointer technique where the physical address of the first card on a row need not be adjacent to the address of the last card on the previous row.



SCREEN

This technique affords an easy implementation of the solution whereby only a small segment of a larger area is currently visible and the screen area may be manually or automatically scanned or panned across the large general area.

The efficiency of this technique is especially valuable in allowing complex fixed patterns to be read directly from the cartridge ROM. This is most visible in "map" type displays, i.e., car racing, galactic voyages, exploring caves, etc.

In a similar manner the microprocessor may algorithmically construct patterns within the system RAM in there complete descriptor list and bit pattern format. The video processor chip may then be instructed to extract the appropriate visible image by modifying its address registers.

Required on chip:

1x16 bit first row pointer
1x16 bit row index
1x24 bit current row value (system variable)
1x6 bit row length value
1x6 bit row length counter (system variable)
1x16 bit last row position
1x24 bit or 1x8 bit global address index

The arithmetic unit, ALU, within the video generator will be shared with all other index functions. The computation, apart from row length value will occur during the line flyback period.

Segmented Display Fields

The video processor is configured as a multiple instruction set machine. The selection of current instruction set may be performed by two methods.

A. Line Flyback Access

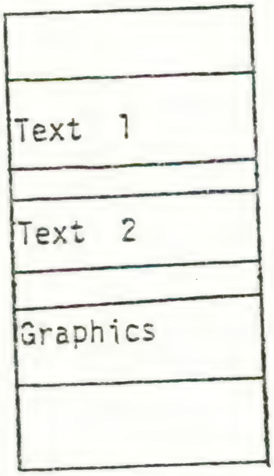
During the non active picture time of horizontal retrace, all row attributes may be modified. This includes the specification of current graphic instruction set.

Note: A possible expansion element would include a dispatch stack within the video generator which may be invoked by using an assigned code within the control area of the descriptor word.

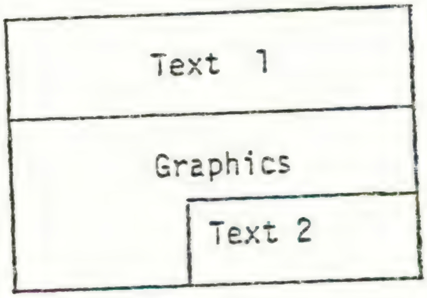
B. Display List Access

During active picture time the system becomes dedicated to supporting the two background pages plus the abundance of foreground objects. It is desirable to include somefacility which allows the firmware to easily select a new graphic instruction set.

The proposed scheme would use one character position to provide the required link value. This word is used to select the appropriate instruction set and to reassign the system address pointers. The use of this feature is best considered graphically.



Descriptor List
Main Memory



Screen Image

The choice of screen format is purely arbitrary and multiple "windows" of graphics and text may be created. The shape of a "window" is also arbitrary except that it must contain an integer number of cards. The overhead of using this function is that on every occasion that an instruction change is invoked one card position must be left in background color wash.

This operation provides a macro redefinition of the system control modes.

Note: By increasing the current line buffer to a 24 bit word the implementation of spacing macros is no longer necessary.

The implication of this change effect two areas. The bus bandwidth is increased by twenty five percent to fetch the extra word and the on chip buffers become 40x24 bit arrays.

10. Perspective Feature

The invocation of the "perspective" mode changes the regular sequence of card fetches into a rate controlled feature which may be based upon a line or a point focus. The operation of this function is that cards "grow" at a variable rate depending upon their distance from the focus. The rate of offset or apparent movement is also a function of the relative distance from the focus.

This feature is of major value in elevation axis motion games, (space travel, auto racing, flying, etc.). The use of special hardware within the video generator unburdens the perspective problems from the system microprocessor and greatly improves the speed of executing this complex function.

11. Two Independent Video Outputs

The video processor chip internally contains eighteen video bit pattern shift registers. A common division of this resource would allocate eight foreground object registers and one background register to be assigned to each video output. It is possible however to assign any combination of the eighteen registers to any output including common definition where a register will output on both ports.

The purpose of the dual output configuration is to permit two television receivers to be used simultaneously. The concept of separate screen images for battle games, strategy situations, etc., clearly illustrate the value of a separate display implementation.

Foreground Object Features

1. Hardware support for 16 individual, reusable foreground objects.

2. Coordinate position resolution on visible plane, 320 horizontal by 192 vertical.

3. Object matrix definition 8x8 to 16x16 in simplex mode, n by n in linked mode.

4. Alternative object definition, based upon a counter configuration instead of a direct bit pattern.

5. Multiple colors per object; 2, 4, 8 per object available.
   The 4 color option is default with one color usually being "transparent"

6. Character pattern available from system ROM or RAM,total memory space.

7. Selectable interactive areas on each object.

8. Programmable pixel clock rate provides smooth, progressive X, Y zoom.

9. Interaction detection based upon a touch algorithm which is executed by the video processor during vertical retrace period.

Detailed Explanation

1. Hardware support for 16 individual, reusable foreground objects.

   The foreground object logic is configured in two parts. Within the video processor circuit is a section of dedicated memory which contains X and Y position registers, an object pattern address register and an area of attribute storage. This circuitry operates in real time to fetch the graphic pattern of each object and to position that object on the selected area of the screen.

   The second area of logic is configured in a general microprocessor architecture. For this video processor the instruction area, ALU and control logic are all contained within the processor chip. The data area for variable storage is a relocatable section of the standard part system RAM. The operation of the resident firmware executes a dispatch table function of moving, rotating and animating objects according to variable values stored within a fixed format array contained within system RAM. The sense of touch interaction and hopefully the result of that interaction are also computed by this firmware feature operating on the external memory.

2. Coordinate positon resolution on visible plane, 320 horizontal by 192 vertical.

   The above values relate to the area typically occupied by a background display. The moving objects are allowed to occupy positions outside this area to provide the function of soft eclipse behind the border area.

3. Object matrix definition 8x8 to 16x16 in simplex mode, n by n in linked mode.

   The simplex mode for a foreground object provides pattern formats identical to those available in all background modes. The 16x16 matrix will be the most common implementation.

   The supplementary mode which is available for foreground objects is an n by n feature. A group of foreground objects may be linked together horizontally. In this mode, when the "complex" object is moved,all its links to the less complex objects are automatically adjusted. Hence, only one coordinate position need be altered.
   The vertical height of the object is controlled by an extension to the addressing mechanism and may occupy the total screen height.

4. Alternative object definition, based upon a counter configuration instead of a direct bit pattern.

   This mode interprets the 16 bit graphic pattern codes as a set of four by four bit counter values. The operation of this function is such that start and stop times of two strokes are defined for each horizontal line of the particular object.

5. Multiple colors per object; 2, 4, 8 per object being possible.

The multiple color mode is identical to that available through the background facilities. The major difference with a foreground object is that one color code will normally be assigned to be transparent.

Only the two and four color modes are available with a 16 pixel wide object. For the four color choice, two 16 bit graphic pattern words are required from memory to define one line of the object.

6. Character pattern available from system ROM or RAM, total memory space. Same facility as background implementation. The graphic pattern is accessed through 24 bit address bus.

7. Selectable interactive areas on each object.

By making the linked elements of an object individually interactive, areas of a complex object can be selectively interactive.

8. Programmable pixel clock rate.

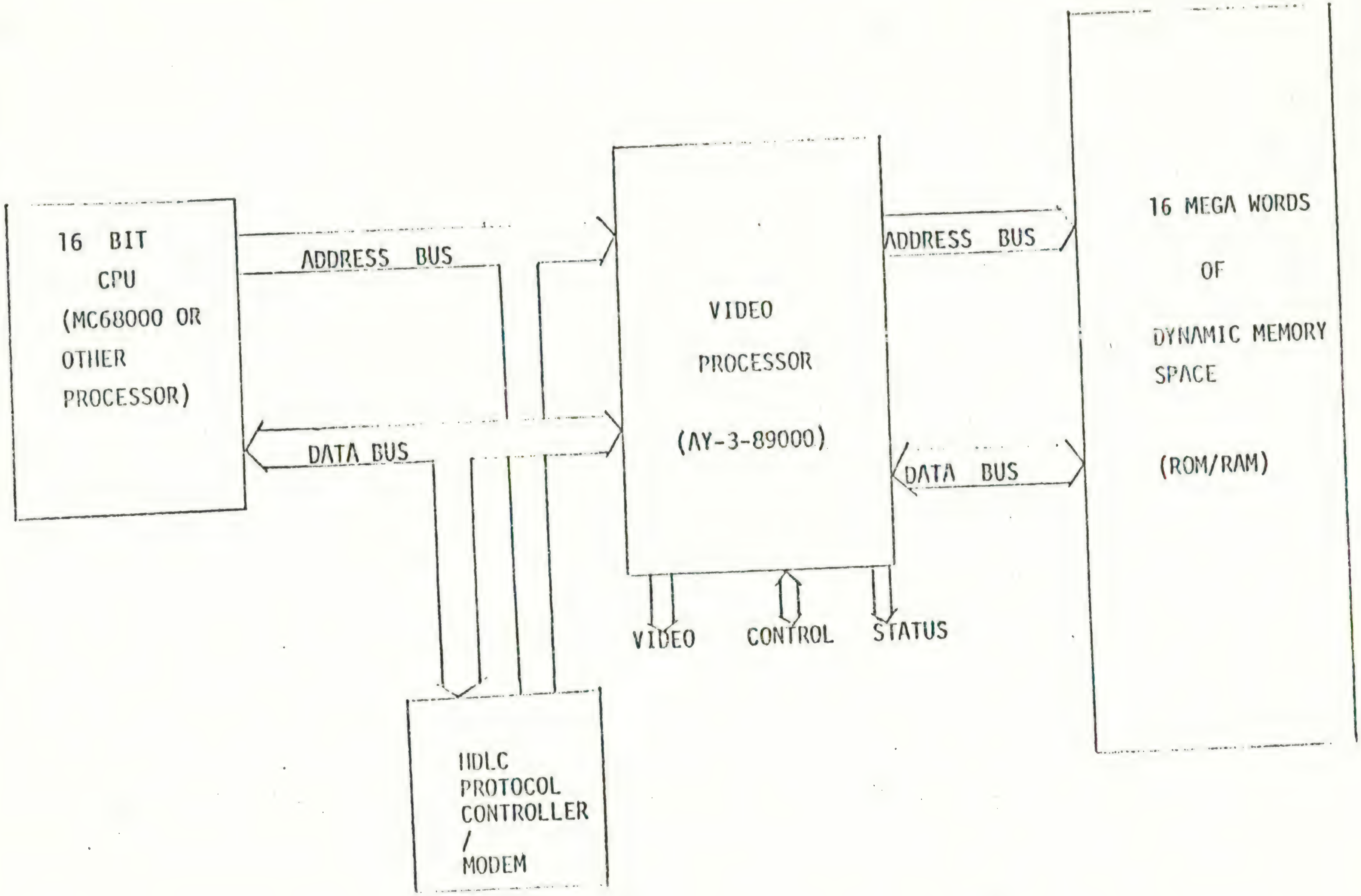
This feature is used to provide a smooth X and Y zoom. The logic is based upon a binary rate multiplier. Very small objects will initially not zoom smoothly.

9. Interaction detection.

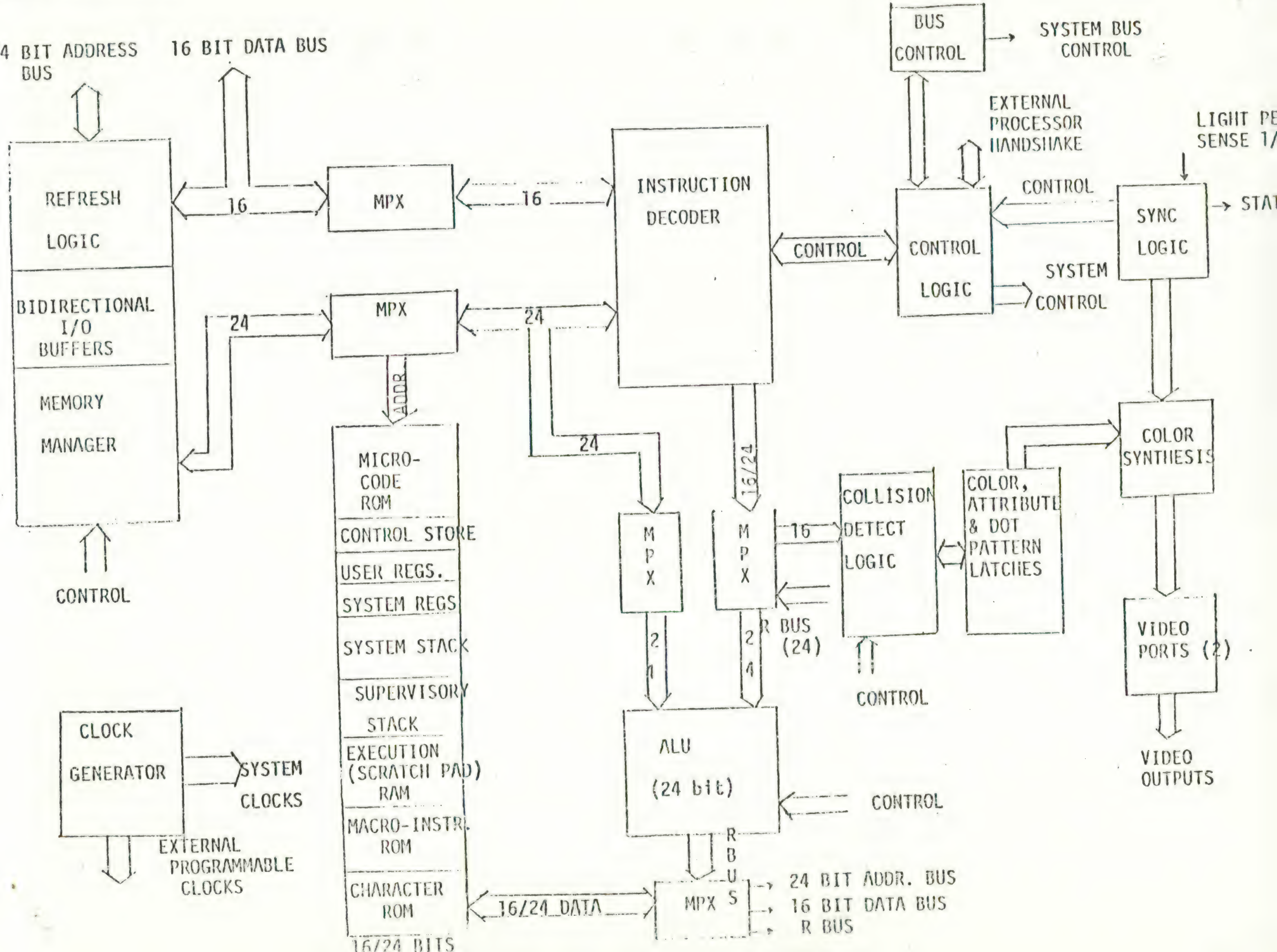
The implementation of this function is completely different to that employed by any current video processor circuit.

With this design we have linked the high performance processor architecture of the chip, to a small area of resident firmware which executes a touch sense algorithm on all moved objects. This algorithm executes during the non video period of vertical retrace. The touch feature, compared to the common video overlap implementation greatly reduces the concidence of software bugs caused by objects becoming buried or trapped within other complex objects. The algorithm will probably execute on a two times shrink of an object which may occasionally sense a touch where there is a one pixel gap. This is entirely satisfactory and presents no hardware or software problem.

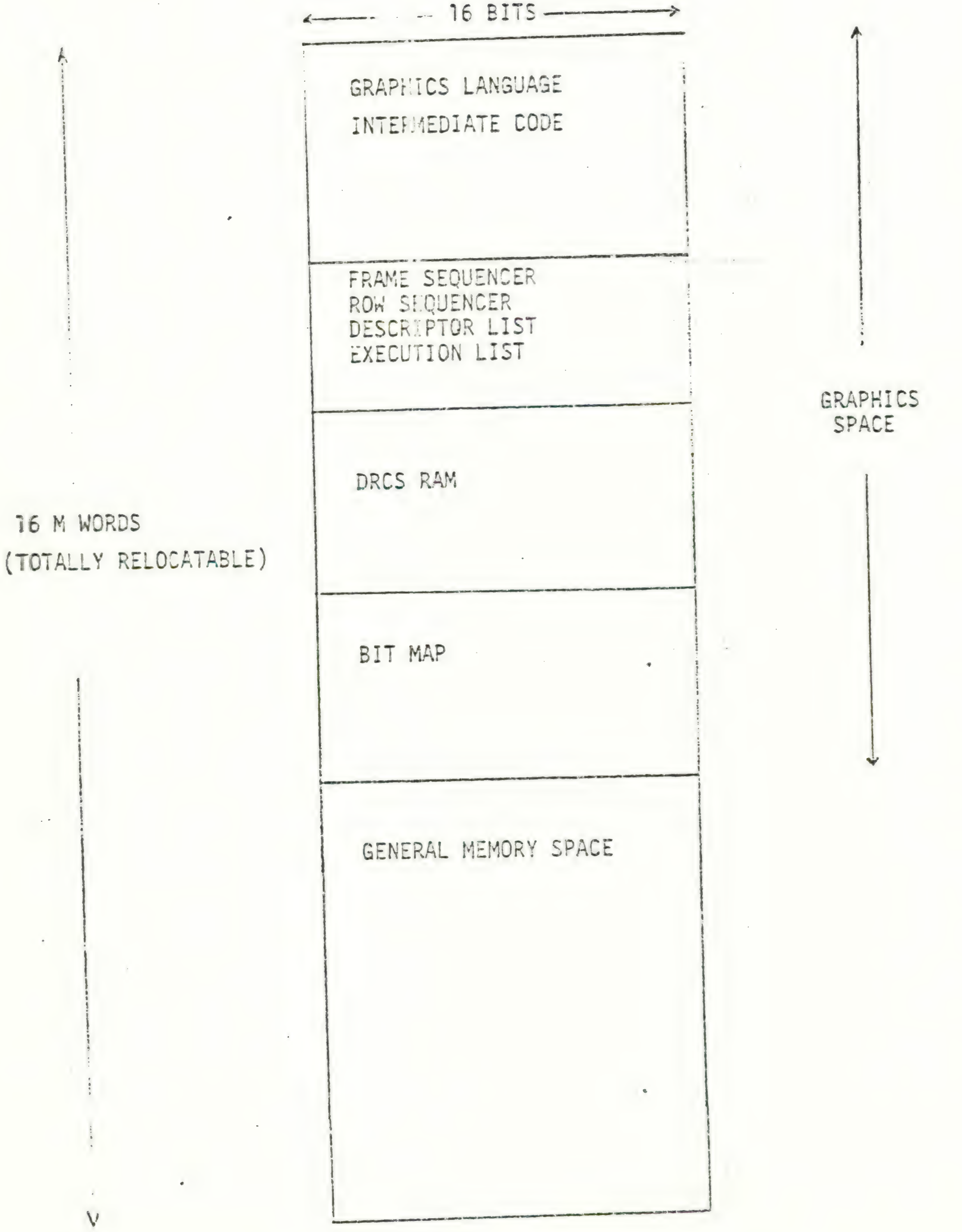
TEM ARCHITECTURE



HIP ARCHITECTURE



ORY ORGANIZATION



GENERAL INSTRUMENT

MICROELECTRONICS GROUP

ADVANCED VIDEO PROCESSOR

AY-3-89000

VIDEO PROCESSOR SYSTEM FEATURES :

- MODULAR DESIGN TO SERVE DIFFERENT SYSTEM APPLICATIONS

- SUPPORTS 3 "FORMS OF LIFE"
  - TEXT BASED PERSONAL AND BUSINESS TERMINAL
  - GAMES ORIENTED SYSTEM
  - PERSONAL COMPUTER SYSTEM

VP SYSTEM FEATURES (continued)

- AT THE PRESENTATION LAYER SUPPORTS :
  - ALPHA-NUMERIC DISPLAYS
  - MOSAIC GRAPHICS
  - DRCS GRAPHICS
  - BIT MAP GRAPHICS
  - GEOMETRIC (PDI) PRIMITIVES
  - OBJECT-ORIENTED GRAPHICS (VIDEO GAMES)
- "CARD" BASED SYSTEM
- CAPABILITY TO OVERLAP PICTURE AND COMPUTER GENERATED GRAPHICS

VP SYSTEM FEATURES (continued)

- PERFORMS AS A SPECIALIZED 16 BIT MICROPROCESSOR
  - EXECUTES GENERAL PURPOSE INSTRUCTIONS
  - COMPILER FOR A "FUNCTIONAL" GRAPHICS LANGUAGE

- ON-BOARD REFRESH LOGIC TO SUPPORT DYNAMIC RAM

- ON-BOARD MEMORY MANAGER
  - PERMITS SYMBOLIC ADDRESSING
  - PROVIDES PROTECTION FOR ALL SEGMENTS OF MEMORY
  - PERMITS RELOCATABLE CODE

- 24 BIT ADDRESS BUS

- 16 BIT DATA BUS

SYSTEM DETAILS

- VP HAS A UNIQUE DUAL FUNCTION ARCHITECTURE
  - EXECUTES AS A 16 BIT MICROPROCESSOR OVER THE FRAME FLYBACK
  - PERFORMS AS A HIGH SPEED VIDEO GENERATOR OVER THE ACTIVE DISPLAY PERIOD
  - COMBINED PROGRAM AND DATA SPACE

- SYSTEM CPU COMMUNICATES WITH VP IN FUNCTIONAL TERMS THROUGH :
  - AN INTERMEDIATE GRAPHICS LANGUAGE
  - A DESCRIPTOR LIST

SYSTEM DETAILS (continued)

- TRANSFORMATION FROM A FUNCTIONAL GRAPHICS LANGUAGE TO THE COLORED DOT PATTERN SEQUENCE IS A TWO PASS EVENT
    - PASS 1 : OVER THE FRAME FLYBACK, THE SYSTEM CPU SUPPLIED PROGRAM IS EXECUTED, GENERATING AN INTERMEDIATE DESCRIPTOR EXECUTION SEQUENCE
    - PASS 2 : THIS DESCRIPTOR LIST IS EXECUTED IN REAL TIME TO CREATE THE DOT PATTERN ON THE SCREEN

- INSTRUCTION REPERTOIRE, CONSISTING OF GENERAL PURPOSE AND DEDICATED INSTRUCTIONS PERMIT THE CREATION OF COMPLEX OBJECT ORIENTED GAMES, ANIMATION SEQUENCES, CARTOON TYPE DISPLAYS AND OTHER COMPUTER GENERATED GRAPHICS WITH MINIMUM OVERHEAD ON THE SYSTEM CPU

- ARCHITECTURE PERMITS NON-SPACING ATTRIBUTES AND SWITCH BETWEEN CODING SCHEMES

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SYSTEM DETAILS (continued)

- PROGRAMMABLE SYSTEM BUS CONFIGURATIONS TO ACCOMODATE A WIDE RANGE OF MICROPROCESSORS

- PIPELINE OF ARCHITECTURE PERMITS SYNCHRONOUS COMMUNICATION BETWEEN SYSTEM CPU AND MEMORY EVEN DURING PEAK UTILIZATION BY VP

- MAXIMUM BUS UTILIZATION IS ACHIEVED BY THE VP RELINQUISHING CONTROL OF THE BUS AT EVERY AVAILABLE INSTANCE

- SYSTEM CPU ALWAYS HAS UNCONDITIONAL CONTROL OVER BUS USAGE

- OVER THE ACTIVE DISPLAY PERIOD, WHEN THE VP IS OFF THE BUS, EITHER THE SYSTEM CPU OR THE PROCESSOR SECTION OF THE VP COULD USE IT

- VIDEO MEMORY SPACE AT ANY INSTANT IN TIME IS A SMALL FRACTION OF THE 16M WORD CAPACITY AND HENCE PROVIDES ENOUGH SYSTEM MEMORY FOR THE SYSTEM CPU TO FUNCTION AS A HIGH LEVEL LANGUAGE INTERPRETER

CHIP ARCHITECTURE

- 24 BIT ALU
- 4 INTERNAL BUSSES
  - 24 BIT ADDRESS BUS (OPERAND 1)
  - 16 BIT DATA BUS (OPERAND 2)
  - 24 BIT RESULT BUS
  - 16 BIT CONTROL BUS
- INPUT CLOCK OF 14.3MHz (FOUR TIMES COLOR BURST FREQUENCY)
- DOT CLOCK OF 7.15MHz
- PIPELINE TIME FOR CHARACTER DISPLAY = 1.1usecs.
- ACTIVE DISPLAY TIME PER TV LINE = 44.0usecs.
- ACTIVE DISPLAY PERIOD PER FIELD = 192 TV LINES.
- VERTICAL BLANKING INTERVAL 4.0msec.
- PICTURE RESOLUTION = 320x192 DOTS
- DISPLAY FORMAT = 40x24
- # OF TIME SLOTS PER CYCLE OF PIPELINE = 4

  . . . . . EACH TIME SLOT = 280nanosecs
- TYPICAL MEMORY ACCESS CYCLE TIME = 200nanosecs
- EACH PIPELINE CYCLE PROVIDES AT LEAST ONE TIME SLOT TO THE SYSTEM CPU
- ON-BOARD LINE BUFFERS ARE LOADED OVER THE LINE FLYBACK OF THE FIRST SLICE OF A DISPLAY CHARACTER
- SIZE OF BUFFER = 80x16
- FOR A 8 LINE DEEP CHARACTER, 7 LINE FLYBACKS CAN BE USED BY THE SYSTEM CPU TO ACCESS MEMORY

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CHIP ARCHITECTURE (continued)

- FUNCTIONAL BLOCKS WITHIN CHIP
  - 16 BIT GENERAL PURPOSE REGISTERS
  - 24/16 BIT SYSTEM REGISTERS
  - SYSTEM STACK
  - USER DEFINED SUPERVISORY STACK THAT SUPPORTS RECURSIVE "CALLS"
  - SCRATCHPAD RAM
  - CHARACTER ROM (VIDEO BIT PATTERNS)
  - MICRO-CODE ROM
  - USER DEFINED CONTROL STORE
  - MACRO-"OPERATION" ROM - MICRO-EXECUTION SEQUENCE FOR SPECIAL INSTRUCTIONS
  - OPTIMIZED INSTRUCTION SET
  - COLLISION/TOUCH DETECT LOGIC
  - SYNC LOGIC
  - ATTRIBUTE LATCHES
  - ADDRESS GENERATOR
  - MEMORY MANAGER
  - DYNAMIC RAM REFRESH LOGIC
  - INSTRUCTION DECODER
  - SYSTEM CONTROL LOGIC
  - BUS CONTROL LOGIC
  - COLOR SYNTHESIS LOGIC
  - DUAL VIDEO PORTS

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DISPLAY FEATURES

- CODING SCHEME
  - ALPHANUMERIC DISPLAY - INTERNAL ROM
  - MOSAIC GRAPHICS
  - DRCS GRAPHICS
  - HIGH DEFINITION BIT MAP DISPLAY - AVERAGE # OF PIXELS OF NO COLOR CHANGE IS 4.
  - ALPHA-GEOMETRIC (PDI)
  - SECONDARY CHARACTER SET - EXTERNAL ROM/RAM
- 16 COLORS SELECTABLE FROM A LARGE COLOR PALLETTE
- 16 REUSABLE MOVING OBJECTS
- PROGRAMMABLE "CARD" SIZE
- PROGRAMMABLE NUMBER OF CHARACTERS PER ROW -40/64/80
- MULTIPLE COLORS IN A CARD
- MULTIPLE VIDEO PLANES
- VISIBLE OBJECT AND VIDEO PLANE PRIORITIES
- OBJECT INTERACTION PRIORITIES
- HORIZONTAL AND VERTICAL DOT (SOFT) SCROLL SELECTABLE ON A FRAME, VIDEO PLANE, ROW OR WINDOW BASIS
- PROGRAMMABLE POSITIONING OF IMAGES IN MEMORY ONTO SCREEN (START OF DISPLAY PERIOD IS SELECTABLE)
- SELECTABLE "PANNING" AREAS
- VARIABLE EXPANSION, CONTRACTION OF OBJECTS OR "BLOCKS" OF MEMORY DEFINING A SHAPE
- MACRO-OPERATIONS PERFORMED ON OBJECTS LIKE ROTATION, TRANSLATION, ETC.

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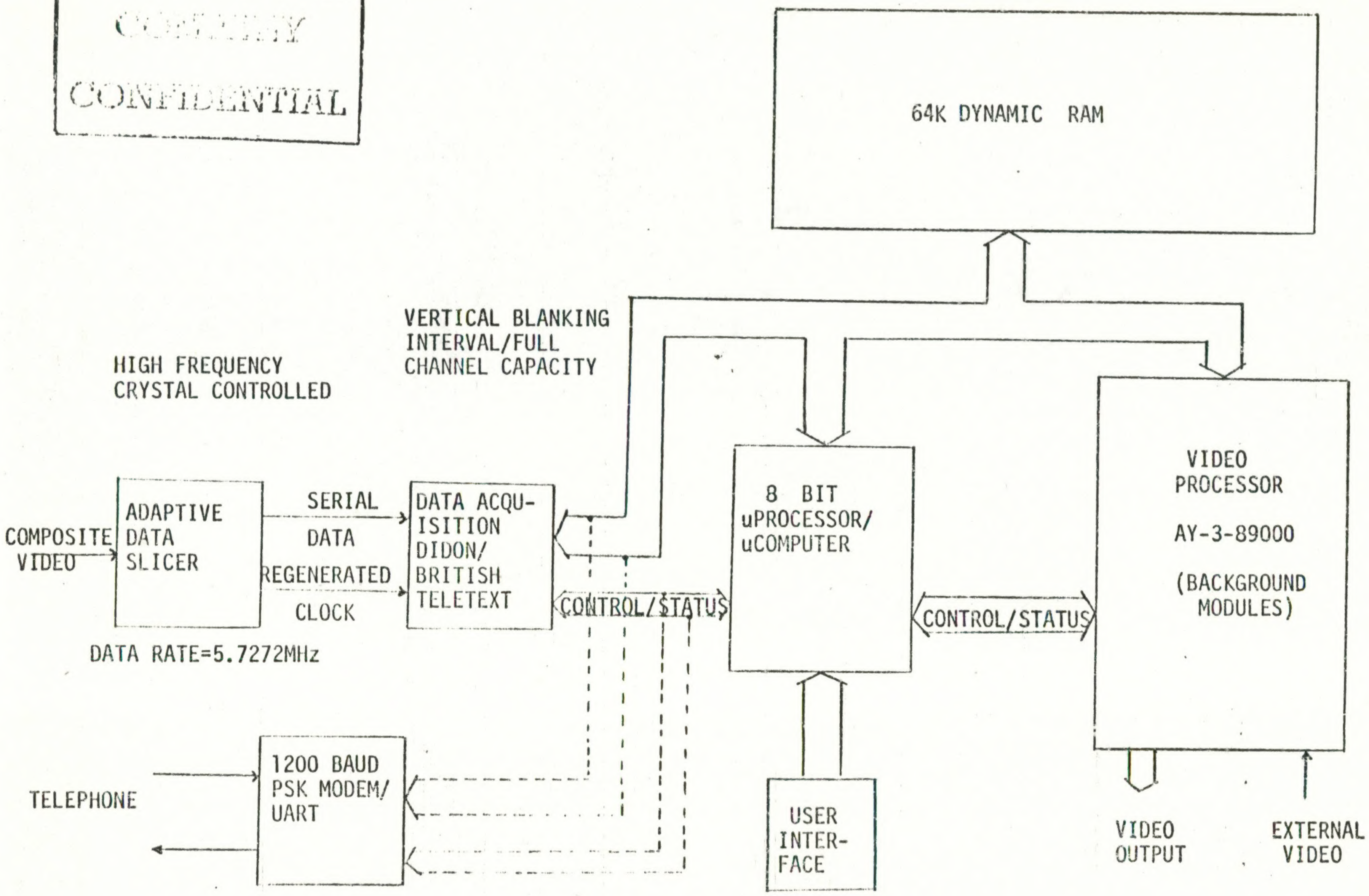
DISPLAY FEATURES (continued)

- A PERSPECTIVE POINT OR LINE OF VISION CAN BE DEFINED, WHICH BECOMES THE REFERENCE AGAINST WHICH OPERATIONS ARE PERFORMED.
- DUAL VIDEO OUTPUT PORTS
- COMPUTER GENERATED GRAPHICS THAT IS A.T.&T. AND PRESTEL COMPATIBLE
- INTERLACED/NON-INTERLACED OPTION
- LIGHT PEN INPUT IDENTIFIES THE SCREEN GRID POSITION
- MULTIPLE DISPLAY FRAMES

FURTHER DETAILS

- FOR OBJECT-ORIENTED DISPLAYS, THE CPU FURNISHED INTERMEDIATE CODE SPECIFIES:
  - OBJECTS TO BE USED FOR CURRENT FRAME
  - CHARACTERISTICS OF OBJECT LIKE:
    - LINKS NEEDED TO CREATE OBJECT
    - VISIBLE PRIORITY OF OBJECT
    - INTERACTION PRIORITY OF OBJECT/LINKS
  - OPERATIONS TO BE PERFORMED ON OBJECTS
  - OPERATIONS REQUIRED FOR ANIMATION SEQUENCES ON "BLOCKS" OF MEMORY REPRESENTING A SHAPE
  - COURSE OF ACTION TO BE TAKEN FOR OBJECTS INTERACTING WITH EACH OTHER
  - ROW/FRAME/WINDOW ATTRIBUTES
- BY MAINTAINING A DIRECTORY AND "RECORDLIKE" DATA STRUCTURES,THE VP COMPILES AN INTERMEDIATE DESCRIPTOR LIST.
- USING A RICH SET OF ADDRESSING MODES, THE VP WALKS ITSELF THROUGH VARIOUS SEGMENTS OF DESCRIPTOR MEMORY, EXECUTING DATA AND INSTRUCTIONS.

TYPICAL TELETEXT/VIEWDATA CONFIGURATION


64K DYNAMIC RAM
VERTICAL BLANKING INTERVAL/FULL CHANNEL CAPACITY
HIGH FREQUENCY CRYSTAL CONTROLLED
COMPOSITE VIDEO
ADAPTIVE DATA SLICER
SERIAL DATA
REGENERATED CLOCK
DATA ACQUISITION DIDON/ BRITISH TELETEXT
DATA RATE=5.7272MHz
CONTROL/STATUS
8 BIT uPROCESSOR/ uCOMPUTER
CONTROL/STATUS
VIDEO PROCESSOR AY-3-89000 (BACKGROUND MODULES)
TELEPHONE
1200 BAUD PSK MODEM/ UART
USER INTER-FACE
VIDEO OUTPUT
EXTERNAL VIDEO

CHIP ARCHITECTURE

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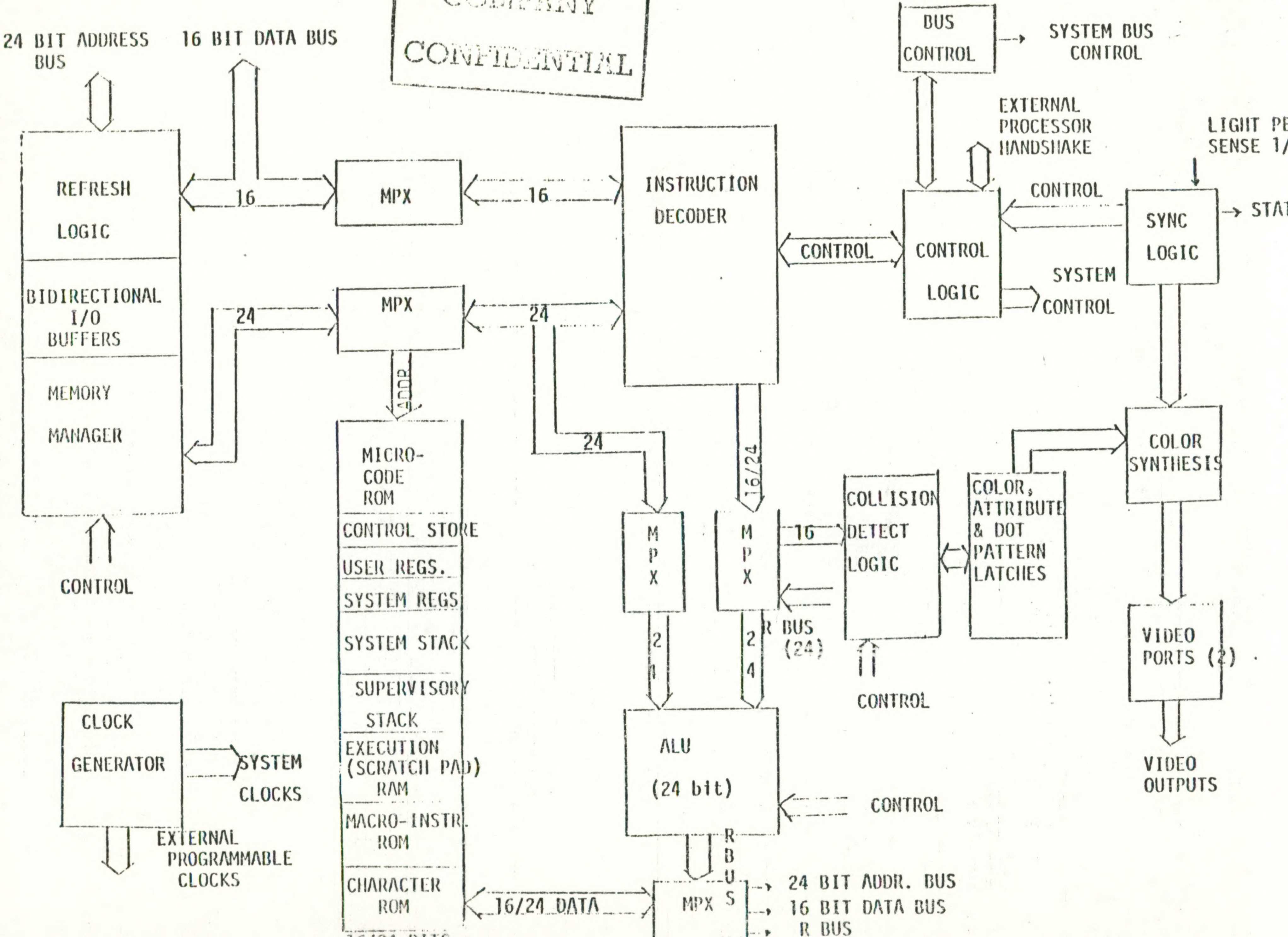
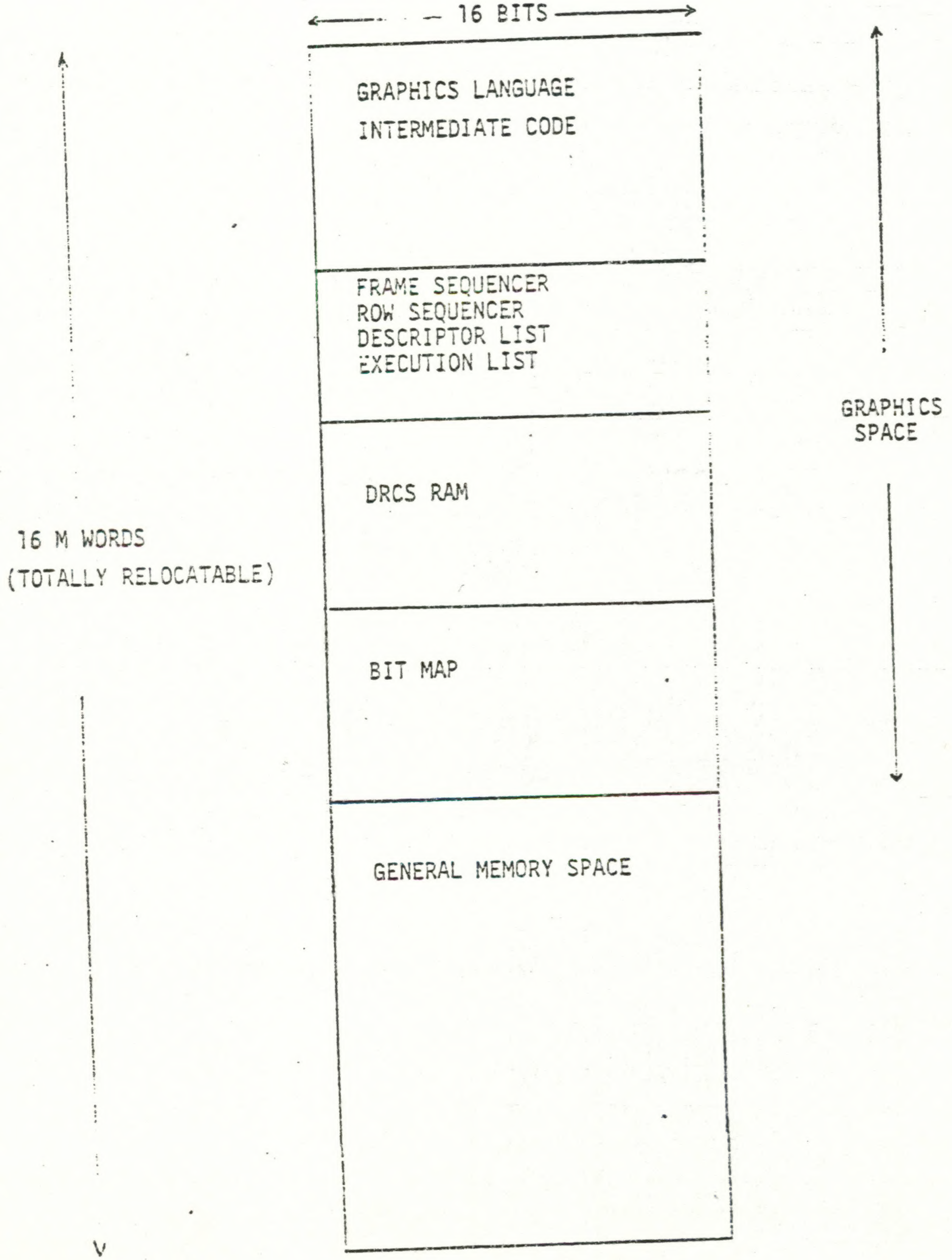
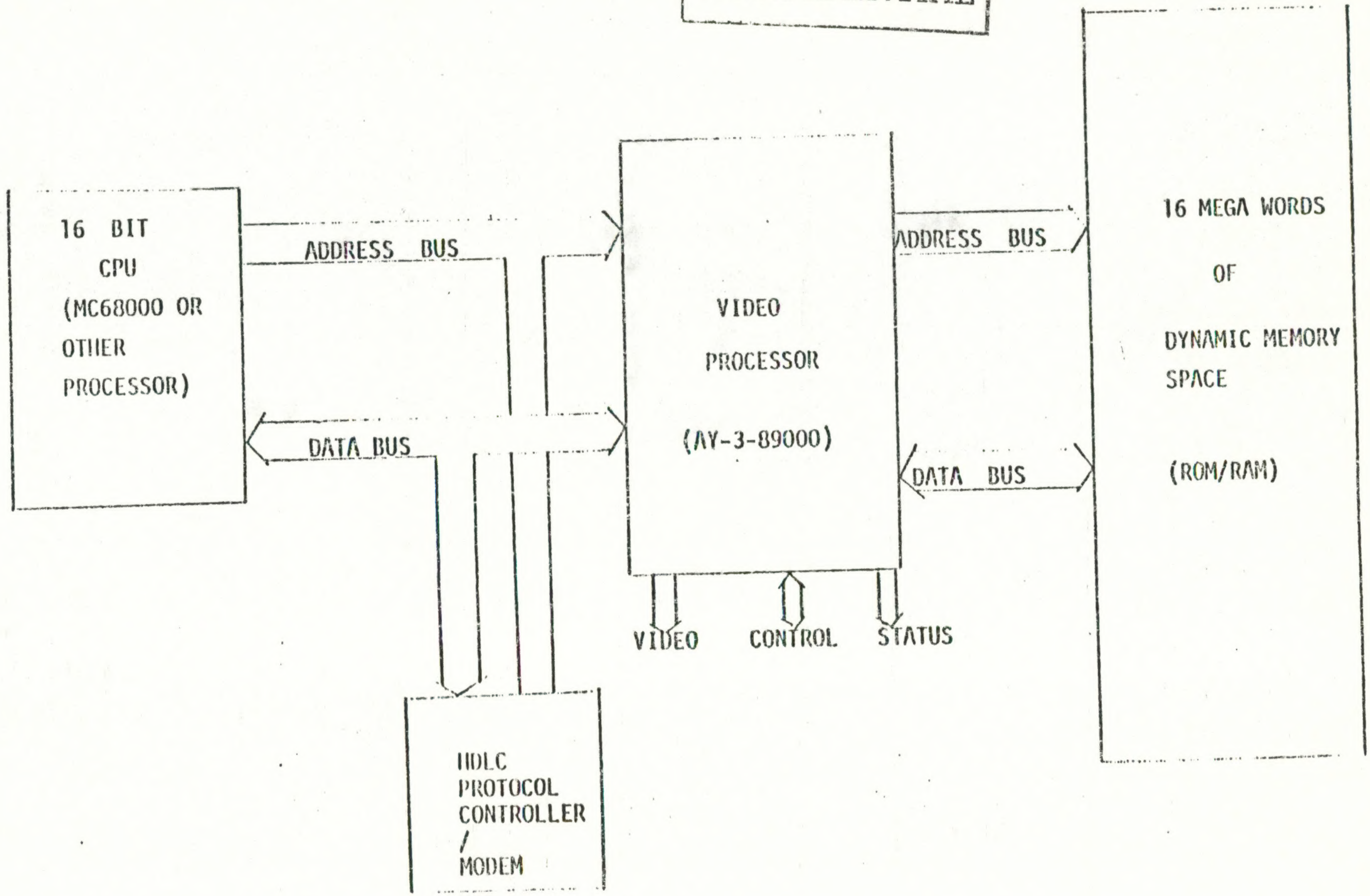


MEMORY ORGANIZATION



YSTEM ARCHITECTURE


16 BIT
CPU
(MC68000 OR
OTHER
PROCESSOR)
ADDRESS BUS
DATA BUS
VIDEO
PROCESSOR
(AY-3-89000)
VIDEO
CONTROL
STATUS
ADDRESS BUS
DATA BUS
16 MEGA WORDS
OF
DYNAMIC MEMORY
SPACE
(ROM/RAM)
HDLC
PROTOCOL
CONTROLLER
/
MODEM